WHAT IS CLAIMED IS:

1. A one time programmable memory circuit comprising:

a one time programmable memory;

a write circuit providing data to the one time programmable memory;

a power up write controller providing the data and a write enable signal to the write circuit;

a read circuit outputting data from the one time programmable memory upon a read enable signal from a read controller; and

an address decoder providing an address to the one time programmable memory for reading to and writing from the one time programmable memory.

2. The circuit of claim **1**, wherein the power up write controller includes:

a power up detection circuit;

an address counter connected to the power up detection circuit and providing the address;

a secure address value detector; and

an address compare circuit providing the write enable signal.

3. The circuit of claim **1**, wherein bits of the one time programmable memory that contain a secure key are not programmed until power up.

4. The circuit of claim **1**, wherein bits of the one time programmable memory that contain a secure key power up at approximately the same rate as power supply rails.

5. The circuit of claim **1**, wherein bits of the one time programmable memory that contain a secure key consume approximately the same amount of current powering up to logical 1 and down to logical 0.

6. A one time programmable memory circuit comprising:

a one time programmable memory;

a power up write controller providing data and a write enable signal to the one time programmable memory;

a read circuit providing data from the one time programmable memory; and

an address decoder providing an address to the one time programmable memory when the address is not a secure data address.

7. The circuit of claim **1**, wherein the power up write controller includes:

a power up detection circuit;

an address counter connected to the power up detection circuit and providing the address;

a secure address value detector; and

an address compare circuit that provides the write enable signal when the address is not a secure data address.

8. The circuit of claim **7**, wherein bits of the one time programmable memory that contain a secure key are not programmed until power up.

9. The circuit of claim **7**, wherein bits of the one time programmable memory that contain a secure key power up at approximately the same rate as power supply rails.

10. The circuit of claim 7, wherein bits of the one time programmable memory that contain a secure key consume approximately the same amount of current powering up to logical 1 and down to logical 0.